Flip Chip Design of Dual Band/Tri mode SiGe BiCMOS Transmitter IC for CDMA Wireless Applications

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Abstract –**Flip Chip circuit design for highly integrated transmitter IC for CDMA handset is presented. The RF flip chip implementation uses peripheral I/O bumps pattern and internal ground bumps within the die, directly on the top metal layer. The IC transmitter is designed to deliver 8 dBm in CDMA mode in cellular band, 11 dBm in AMPS mode and 9 dBm in CDMA mode in PCS band at 90 , 88, 108 mA, respectively. Results show that flip chip implementation meets or exceeds the wirebond RFIC performance.**

I. INTRODUCTION

Reduction in cost and size are the main driving for all the furious development activities in RFIC transceivers. At the same time, more stringent system performance requirements impose new challenges for the design and implementation of these highly integrated RFIC. For cost reduction, Silicon (Si) RFIC have been adopted for higher frequency applications using SiGe process. For size reduction and better performance at high frequency, Flip Chip (FC) RFIC in Chip Scale Package (CSP) is used, especially to improve the isolation on low resistivity Si substrate [1].

In this paper, FC implementation of highly integrated dual band, tri-mode transmitter IC for CDMA handset compliant with the TIA/EIA 98-D applications is presented [2]. This highly integrated IC eliminates the need for SAW filters in the transmit path, and integrates both VHF and UHF PLL without imposing any penalty on the current consumption and die size. The transmitter RFIC is fabricated on Jazz semiconductor 0.35 um SiGe BiCMOS process, and packaged in a 6x6 mm Land Grid Array (LGA) package. As first implementation for FC application, the wirebond version of the transceiver has been implemented using FC technology in the same package size. The goal of this work is to achieve the specifications and establish design guide lines for FC development. The circuit design is slightly optimized to account for the new flipped die environment, and the package parasitics are adjusted to account for the difference between the wirebond and flip chip implementation.

II. Why RF Flip Chip?

RFIC at around 2 GHz has been successfully implemented using wirebond technology [2]. However, Flip Chip provides a long tem potential alternative for significantly reducing package costs and system size using Direct Chip Attach (DCA) to PCB system boards. High system pin counts in highly integrated IC is also possible using Re-Distribution Layer (RDL). FC also offers improved performance and noise margin for RF, digital and mixed signal applications in highly integrated die,

- low AC impedance signal paths due to inductance drops from nHs' in Wirebond (WB) to pHs' in FlipChip and flexibility in adjusting the package parasitics using the package line interconnects,
- low impedance bias and ground paths, and bounce improvements, especially when Power supply and Ground are provided close to noisy circuits,
- potential improvement in signal noise coupled through substrate due to less noise injection and more efficient collection of substrate stray shallow and deep charges

are all advantages that facilitate the System-On-Chip (SOC) implementation and improve the available design margin.

RF flip chip imposes limitations on the use of RDL because longer and inconsistent signal path lengths may affect circuit timing and/or noise coupling. In addition, coupling between RDL and die components is difficult to predict and model. Finally, RFIC are cost sensitive product and the use of RDL implies increased die cost with extra process steps for additional metal and dielectric layers. At the same time, there are many challenges relative to noise reduction using flip chip. First, low impedance power supply and ground must be provided

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close to noise generator in circuit, so bump pads must be placed inside the circuit layout in RF FC, as will be shown later. Solid ground planes for digital/mixed signal and RF may require increased number of package VIAS that might be competing with bumps in real state. Signal interaction between bump pads and underlying circuit components must be also taken into consideration. Fig. 1 shows simulated results for low loss Si substrate noise coupling comparison between FC and WB using Substrate Storm. The guard ring is grounded through bumps in case of FC and wirebond in case of WB. The probing ports are placed at upper left and middle right of the circuit. Results show that deep carrier injection is reduced and led to 8 dB isolation improvement at 2 GHz and 30 dB at 8 GHz. The enhancement is primarily due to lack of bottom grounded die substrate with FC. The reduction in ground impedance also leads to non dispersive behavior of the coupling through Si substrate.

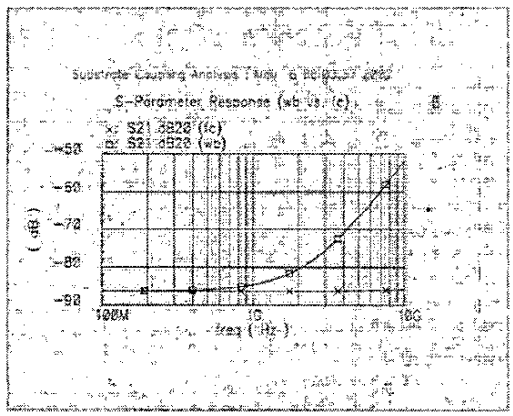


Fig. 1 Isolation comparison in low loss Si substrate between FC and WB circuit environment.

Cost is crucial in technology trade-off and implementation, especially in High Volume (HV) products. The reduction in package cost for FC compared to WB, due to lower cost in assembly materials and overhead should offset the increase cost of bumped Si wafers, without RDL. This may lead to reduction in the final cost of HV FC product compared to wirebond, assuming same front-to-end yield for both FC and WB products.

III. RF FC CIRCUIT DESIDN CONSIDERATIONS

Highly integrated RFIC products require relatively low number of I/O signals, which are about the same as package pins, and large number of ground downbonding. Fig. 2 presents number of I/O signal counts versus die size for typical RF products as function of FC bump pitch in different configurations. It is clear that peripheral bump can fit most of the typical RF highly integrated products, assuming all ground bumps are placed in the middle of the die.

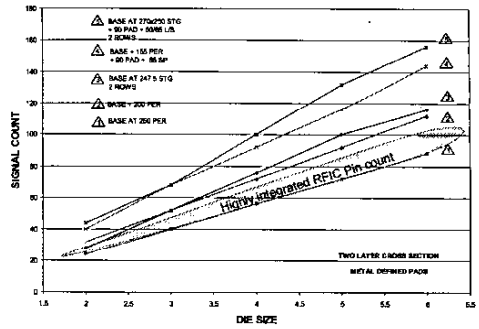


Fig. 2 I/O signal counts versus die size for typical as function of FC bump pitch.

RF Si wafer process is characterized by its thick top metal layer 2-3 um with its uneven passivation pattern. Also, inductor and baluns on die have 1-2 um separation between metal lines. High Q MIM capacitors are embedded between Metal 2 and Metal 3 in 3 metal layers process. Finally, ESD in RF FC might be placed at the center of the die. All of these factors may require special considerations when designing on RF FC technology. Experimental results at wafer process and bump houses, plus Skyworks show that cost and yield are not affected.

FC HV RFIC bump pattern proposed in this work is peripheral bumps for I/O and non uniform but nearly symmetric distribution for center inner bumps. This configuration will require the use of both Metal Defined Pad (MDP) and Solder Mask Defined Pad (SMDP) in the same design. For mixed design, bump pad opening should be optimized to ensure constant bump height and die planarity. In addition, inner bump pitch should be similar to staggered bump pattern with pitch larger than the peripheral bump pitch to avoid void under the die. Fig. 3 shows an example for the bump pattern configuration.

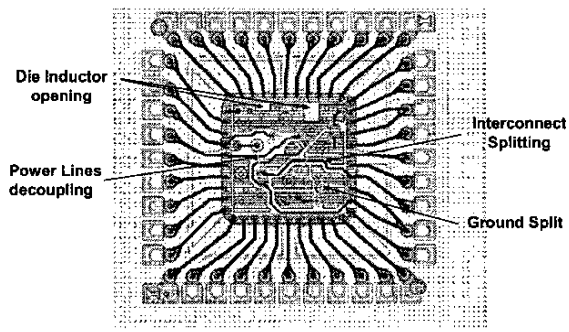


Fig. 3 Bump pattern distribution for RF flip chip, and FC package layout.

The on-die inductors and baluns performance will be affected by the ground plane facing the die in FC environment. Modeling and characterization for these passive components in the new flip chip environment become critical to properly predict the circuit performance.

Circuit design and layout should be performed concurrently for IC/Package design. To fully take advantage of FC, true IC/Package codesign is required. The package becomes an integral part of the circuit design.. Several techniques can be used to enhance the design, as ground splits and mixed interconnects, as shown in Fig. 3. Finally, mixed passive between die and package can be implemented, as in inductance and baluns. Ground shielding techniques underneath sensitive circuit is also possible [1].

Fig.4 depicts the implementation of ground bumps within the die circuitry. It can be observed that the bump dimension compared to on-die balun is small. The bump in this case can be placed in the isolation unused area around baluns and inductors. For relatively large by-pass capacitor, the top metal layer can be used for die bump pad, which also provides the shortest path to ground.

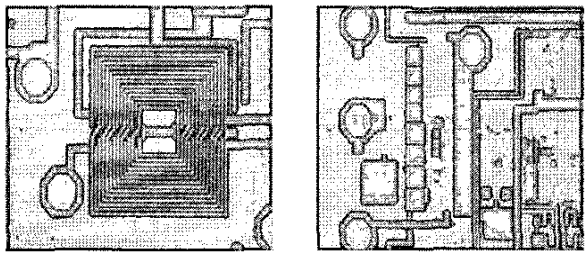


Fig. 4 Ground die bump pad distribution within the die circuitry.

IV. TRANSMITTER RFIC BLOCK DIAGRAM

The transmitter IC is designed as dual-up converter architecture with gain control distributed appropriately between the IF and RF stages, and its block diagram is shown in Fig.5. The IF section upconverts the I/Q analog baseband signals, using I/Q modulator, to IF signal which is fed to a Voltage Gain Amplifier (VGA) that provides the IF gain as well as 80 dB of power control. The filtered IF signal is first upconverted by image reject mixer to RF frequency in cellular or PCS band. The RF signal is then fed to RF Power Amplifier (PA) drivers that provide the required power level in the desired frequency band for external PA. One cellular PA driver and two PCS PA drivers are provided. Integrated baluns are utilized to convert the differential RF signal to single ended signal that is required by the SAW filter between the PA drivers and the PA. The IC includes two integer-N PLLs necessary for VHF and UHF frequency bands to enable the frequency control of the integrated internal VHF and the external UHF VCOs.

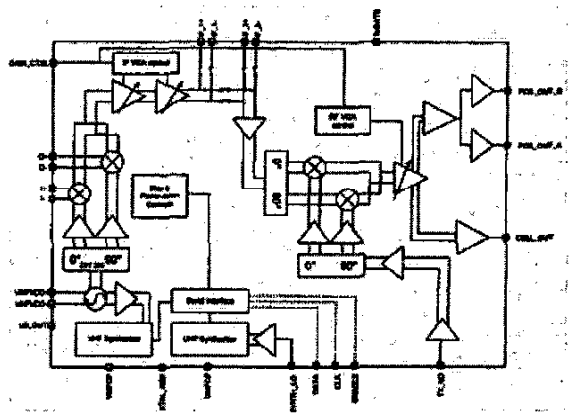


Fig. 5 Simplified block diagram of the IC CDMA transmitter.

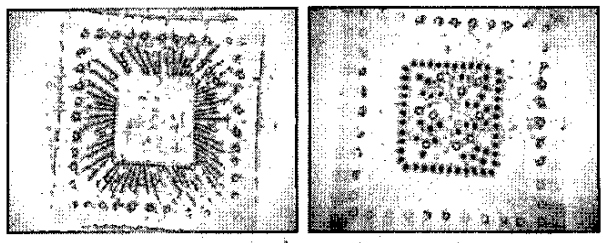
V. MEASURED RESULTS

The transmitter IC has been designed on SiGe BiCMOS for WB and FC packaging technology. The WB and FC dice are implemented on the same wafer and both LGA packages are developed using the same package substrate to reduce the effect of process variations on the measured results. Both dice and both packages have exactly the same dimensions, as shown in Fig. 6. The FC die circuit and FC package substrate has been designed concurrently and optimized for the new FC environment. This design does not necessarily take full advantage of FC technology, since the goal of this work is to achieve the specifications and establish design guide lines for FC development using the same infrastructure available for the WB version. The WB and FC designs use the same evaluation board and same ATE fixture with no extra tuning.

Measured results on both evaluation board, depicted in Fig. 7 and 8, and ATE fixture, presented in Table 1, show that FC and WB implementation meets the design SPECs. Cell_LO_Leakage in FC is about 20 dB better than WB, so better isolation can be achieved using FC. Also, PCS ACPR in FC is about 2 dB greater than WB at the same power level. Finally, results show that no change in leakage current with FC, so bump mechanical interaction, even at the middle of the die, with RF FC die is negligible.

VI. CONCLUSION

Low cost RF flip chip circuit design for highly integrated transmitter IC for CDMA handset is presented.



(a) Wirebond (b) Flip Chip

Fig. 6 CDMA RFIC transmitter X-ray pictures

The design uses peripheral bumps and internal bumps within the die pattern to reduce the die size. Design guide lines for RF FC circuit design have also been developed. Results show that FC implementation meets or exceeds the wirebond RFIC performance, especially in isolation and linearity.

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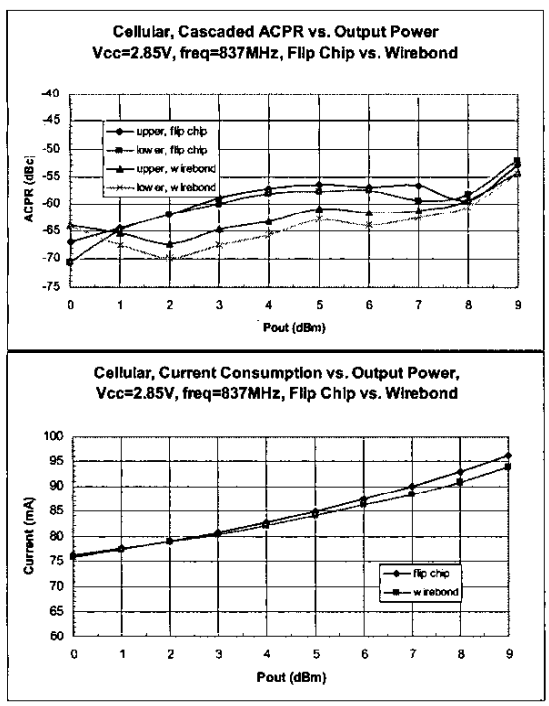

Fig. 7 Cellular ACPR and DC Current for FC and WB

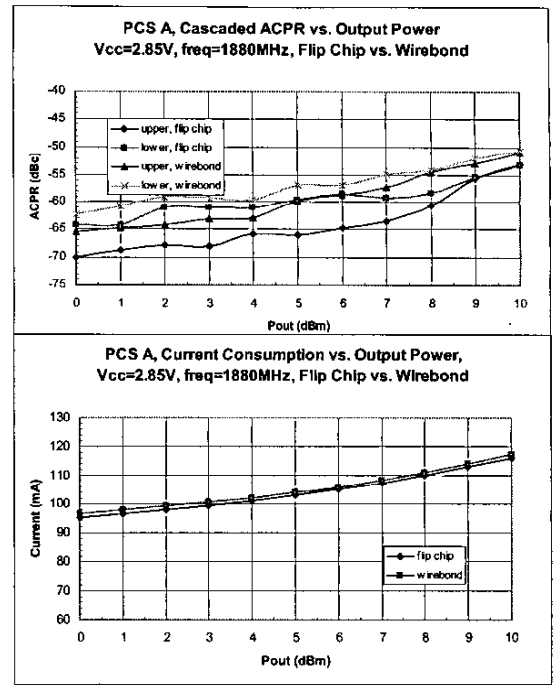

Fig. 8 PCS ACPR and DC Current for FC and WB

Table 1. ATE measurement for FC and WB

Performance	FC	WB	Conditions
Pout (dbm)	12.91	13.60	AMPS
Pout (dbm)	11.15	11.35	CDMA
Pout (dbm)	11.82	12.56	PCS A
APCR	-57.76	-58.76	Cellular
APCR	-55.01	-53.69	PCS A
LO leakage at RF	-57.49	-21.56	Cellular
Sleep current(uA)	46.50	46.60	
Current (mA)	115.60	114.70	AMPS
Current (mA)	74.00	79.00	CDMA
Current (mA)	88.40	93.90	PCS

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